wherein the penetration hole is formed at a position according to a matrix, and wherein said IC chip is coupled directly with said ground layer.

35. (Amended) A module component according to claim 1, further comprising a dummy component disposed in another penetration hole of said penetration holes, said dummy component having a size almost the same as said chip components and functioning as an insulator.

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claims 1, 8, 10, 12 and 31-35 so as to address the claim objections set forth in paragraph 1 of the Office Action and to further distinguish the present invention over the cited prior art reference. For the reasons set forth below, it is respectfully submitted that all pending claims are patentable over the cited prior art.

Applicants would like to thank the Examiner for the indication of allowance of claims 10-12 and 31-35.

Further, it is noted that with regard to the claim objections concerning claims 8, 10, 12 and 31-34, the claims have been amended to change "a circuit wiring" to "circuit wiring" as suggested by the Examiner. However, as each of these claims recites a single penetration hole, the Applicants have not changed "a chip component" to "chip components, each" as requested as it believed that such a change is not necessary. If

for any reason upon review the Examiner believes the change is required, the Examiner is respectfully requested to contact the undersigned attorney to discuss the issue in further detail.

II. The Rejection Of The Claims Under 35 U.S.C. § 102

Claims 1, 4, 6, 7 and 9 were rejected under 35 U.S.C. § 102 as being anticipated by USP No. 4,979,076 to DiBugnara. Applicants respectfully submit that, as amended, the foregoing pending claims are clearly not anticipated by DiBugnara.

As recited by amended claim 1, referring to Fig. 3a of the specification, the plurality of penetration holes are disposed so as to form a matrix of aligned rows and aligned columns of penetration holes. As recited by amended claim 1, ***each penetration hole is contained in at least one row and one column of the matrix, and each row and each column of the matrix includes at least two penetration holes***. As result of the formation of such a matrix, the insertion of the chip components into the penetration holes can be performed precisely and in a rapid manner, thereby providing a reduction in the manufacturing time necessary to form the device and a corresponding cost savings.

In contrast, the device disclosed in DiBugnara, it is clear that the cited prior art does not disclose or suggest the foregoing limitation recited by amended claim 1. For example, referring to Fig. 1 of DiBugnara, while opening 14 is arguable aligned in a row with opening 13, it is clear that opening 14 is not aligned in a column with any other opening. Thus, at a minimum, DiBugnara does not disclose a matrix wherein each

penetration hole is contained in at least one row and one column of the matrix, and each row and each column of the matrix includes at least two penetration holes.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), and, at a minimum, DiBugnara does not disclose the foregoing limitation, it is clear that DiBugnara does not anticipate amended claim 1, or any claim dependent thereon.

III. The Rejection Of Claim 8 Under 35 U.S.C. § 103

Claim 8 was rejected under 35 U.S.C. § 103 as being anticipated by USP No. 4,979,076 to DiBugnara in view of USP No. 5,875,100 to Yamashita. Applicants respectfully submit that, for at least the following reasons, claim 8 is patentable over DiBugnara and Yamashita taken alone or in combination with one another.

As recited by pending claim 8, the present invention relates to a module component comprising in-part: a chip component disposed in a penetration hole, where the chip component has a height which is greater than the depth of the penetration hole, but which does not result in the component projecting from the first and second auxiliary substrates, which are formed on the surfaces of the substrate in which the penetration hole is formed. For example, as shown in Fig. 2 of the specification, the height of the chip component (1005) while being greater than the depth of the penetration hole, is such that the chip component does not project from the first and

second auxiliary substrates (5 and 6).

Turning to the cited prior art, in the pending rejection, it is admitted that DiBugnara does not disclose a chip component having a height greater than the depth of the penetration hole. Yamashita is relied upon as curing this deficiency. It is respectfully submitted that this conclusion is incorrect for at least the following reasons.

First, it is noted that the penetration hole disclosed in Yamashita, which is identified by reference numeral 21 in Fig. 1A and which functions to receive the component 10, does not extend through the entire substrate as recited by the pending claim so as to allow the chip component disposed in the penetration hole to contact circuit wiring disposed on both sides of the substrate. As is clear from the figures of Yamashita, the penetration hole 21 only extends halfway through the substrate. However, the penetration hole of DiBugnara must extend through the entire substrate as shown in Fig. 1 of DiBugnara. Thus, the proposed modification of DiBugnara, which would require the use of the hole 21 of Yamashita, would effectively destroy the intended functionality of DiBugnara, and is therefore improper.

Moreover, based on the fact that the penetration of Yamashita only extends halfway through the substrate, there is simply no motivation to modify DiBugnara with Yamashita as suggested in the pending rejection. As is well known, there must be **objective evidence** supporting the proposed modification. It is improper to simply pick and choose elements from the various prior art references. It is respectfully submitted that there is simply no motivation to make the proposed modification.

Second, as shown in Fig. 3 of DiBugnara, the auxiliary substrates 51 and 61 are

placed directed above the chip component 41. Thus, it does not appear to be possible to modify the device of DiBugnara such that the chip component has a height larger than the penetration hole such that it extends into the planes defined by the auxiliary substrates because, as stated, the auxiliary substrates are formed directly on top of the chip component. Thus, for this additional reason, the proposed modification of DiBugnara as set forth in the pending rejection would defeat the intended functionality of DiBugnara.

As is well known, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, there is no suggestion or motivation to make the proposed modification (*see*, M.P.E.P. § 2143.01).

Accordingly, for at least the foregoing reasons, it is respectfully submitted that the pending rejection based on the combination of DiBugnara and Yamashita is improper and should be withdrawn.

IV. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

V. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 5/5/03

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VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE CLAIMS:

Claims 1, 8, 10, 12 and 31-35 have been amended as follows:

1. (Thrice Amended) A module component comprising:

a substrate made of resin having a plurality of penetration holes, said plurality of penetration holes disposed in said substrate so as to form a matrix of one of aligned rows and aligned columns of the penetration holes, each of said penetration holes being aligned in both a row and a column of said matrix, and each row and each column of said matrix comprising at least two penetration holes;

[a] circuit wiring disposed on both sides of said substrate; and

[a chip component] chip components having a height almost the same as a depth of each of said penetration holes, one of said chip [component] components being disposed in one of said penetration holes for electrically coupling said circuit wiring disposed on both sides of said substrate.

8. (Twice Amended) A module component comprising:

a substrate made of resin having a penetration hole;

[a] circuit wiring disposed on both sides of said substrate; and

first and second auxiliary substrates disposed such that said substrate is disposed between said first and second auxiliary substrates, and

a chip component disposed in the penetration hole, said chip component having a specified height being greater than the depth of the penetration hole and not

projecting from said first and second auxiliary substrates, said chip component electrically coupling said circuit wiring disposed on both sides of said substrate,

wherein the penetration hole is formed at a position according to a matrix.

10. (Twice Amended) A module component comprising:

a substrate made of resin having a penetration hole;

[a] circuit wiring disposed on both sides of said substrate;

a chip component having a height almost same as a depth of said penetration hole and put in the penetration hole for electrically coupling said circuit wiring disposed on both sides of said substrate;

an auxiliary substrate disposed over said substrate;

an IC chip mounted on said auxiliary substrate; and

a capacitor put in said penetration hole immediately beneath said IC chip to be coupled directly with said IC chip,

wherein the penetration hole is formed at a position according to a matrix.

12. (Twice Amended) A module component comprising:

a substrate made of resin having a penetration hole;

[a] circuit wiring disposed on both sides of said substrate; and

a chip component having a height almost the same as a depth of said penetration hole and put in the penetration hole for electrically coupling said circuit wiring disposed on both sides of said substrate;

an auxiliary substrate disposed over said substrate;

an IC chip mounted on said auxiliary substrate; and

a ground layer disposed beneath said substrate,

wherein the penetration hole is formed at a position according to a matrix;

wherein a chip component having a specific value is accommodated to compose a desired circuit; and

wherein said IC chip is coupled directly with said ground layer.

31. (Amended) A module component comprising:

a substrate made of resin having a penetration hole;

[a] circuit wiring disposed on both sides of said substrate;

a chip component having a height almost same as a depth of said penetration hole and put in the penetration hole for electrically coupling said circuit wiring disposed on both sides of said substrate; and

wherein the penetration hole is formed at a position according to a matrix,

wherein a chip component having a specific value is accommodated to compose a desired circuit, and

wherein the penetration hole is tapered.

32. (Amended) A module component comprising:

a substrate made of resin having a penetration hole;

[a] circuit wiring disposed on both sides of said substrate;

a chip component having a height almost same as a depth of said penetration hole and put in the penetration hole for electrically coupling said circuit wiring disposed on both sides of said substrate; and

a ground layer disposed beneath said substrate, said ground layer being coupled with said circuit wiring disposed on a lower side of said substrate,

wherein the penetration hole is formed at a position according to a matrix, and

wherein a chip component having a specific value is accommodated to compose a desired circuit.

33. (Amended) A module component comprising:

a substrate made of resin having a penetration hole;

[a] circuit wiring disposed on both sides of said substrate;

a chip component having a height almost same as a depth of said penetration hole and put in the penetration hole for electrically coupling said circuit wiring disposed on both sides of said substrate;

an auxiliary substrate disposed over said substrate; and

a ground layer disposed beneath said auxiliary substrate, said ground layer being coupled with said circuit wiring disposed on a lower side of said substrate.

34. (Amended) A module component comprising:

a substrate made of resin having a penetration hole;

[a] circuit wiring disposed on both sides of said substrate;

a chip component having a height almost same as a depth of said penetration hole and put in the penetration hole for electrically coupling said circuit wiring disposed on both sides of said substrate;

an auxiliary substrate disposed over said substrate;

an IC chip mounted on said auxiliary substrate; and

a ground layer disposed beneath said auxiliary substrate,

wherein the penetration hole is formed at a position according to a matrix, and

wherein said IC chip is coupled directly with said ground layer.

35. (Amended) A module component according to claim 1, further comprising a dummy component disposed in another penetration hole of said penetration holes, said dummy component having a size almost the same as said chip [component] components and functioning as an insulator.